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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/058,837	01/30/2002	Takashi Okada	61352-016	2419

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EXAMINER	
DI GRAZIO, JEANNE A	

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 08/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/058,837	OKADA ET AL.	
	Examiner	Art Unit	
	Jeanne A. Di Grazio	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 27 May 2004.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-3 is/are pending in the application.

4a) Of the above claim(s) 4-22 is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-3 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

Applicant claims priority to Japanese Patent Application No. 2001-22964 (Jan. 31, 2001).

Claim Objections

Claims 1-3 are objected to because of the following informalities:

As to claims 1-3, the periphery length of the gate electrode to pixel electrode capacitor, designated by Applicant as "Lgd" is not adequately defined in the Specification.

Specifically, Applicant has recited in independent claim 1, "and a periphery length of a gate electrode to pixel electrode capacitor, which is a capacitor formed between the gate electrode of the pixel transistor and the pixel electrode, is Lgd."

The periphery length, Lgd, because it is not adequately defined, may mean any number of possibilities: (1) it may mean the periphery length of the gate electrode section opposed by source and drain electrodes of a thin film transistor, or (2) it may mean the periphery length of the gate electrode section opposed by source and drain electrodes of a thin film transistor in addition to the periphery (or periphery length) of the pixel electrode, or (3) it may mean a cross sectional length of a combination of possibilities (1) and (2) above.

Furthermore, it is respectfully pointed out that periphery means "the perimeter of a circle or other **closed** curve" (Merriam Webster's Collegiate Dictionary 10^{TH} Ed. at page 862)(emphasis added). It appears to the Examiner that a gate electrode to pixel electrode capacitor which Applicant refers to as a *capacitor formed between* the gate electrode of the pixel

electrode and the pixel transistor cannot technically have a *periphery length* since a gate electrode to pixel electrode capacitor appears to be a comparison between the gate electrode to the pixel electrode *capacitor*.

For examination purposes, the Examiner interprets said limitation to mean possibility (1) above.

Appropriate correction is **required**.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe et al. (US 5,691,793) in view of Park et al. (US 6,411,347 B1).

As to claims 1-3, Watanabe has with reference to Figure 1, a signal line(s) that applies a predetermined image signal voltage (Column 7, Lines 65-66)(Applicant's "a plurality of source lines for transmitting a video signal"), a gate connected to a scanning line and the gate and signal lines cross over each other (signal line 5 and scanning line 9)(Column 7, Line 65)(Applicant's "a plurality of gate lines arranged so as to intersect the plurality of source lines in a plan view, for transmitting a gate signal"), a plurality of pixels defined by the plurality of source lines and the plurality of gate lines which intersect each other and constituting an image display plane (See Figure 1), a pixel electrode provided for every pixel (See Figure 1), an opposed substrate (not shown) that has a counter electrode across from a liquid crystal composition (Column 8, Lines 66-67 and Column 9, Lines 1-14)(Applicant's "an opposed electrode facing the pixel electrode across a liquid crystal layer"), storage capacitors (Figure 1, reference item 419) provided for every pixel electrode (Column 9, Lines 37-56)(Applicant's "a storage capacitor provided for every pixel for holding a voltage applied between its corresponding pixel electrode and the opposed electrode"), and TFTs having source 409 and gate 405 and drain 411(Columns 9 and 10)(Applicant's "a pixel transistor provided for every pixel, having a source electrode, a drain electrode, and a gate electrode which are connected to a corresponding one of the source lines, a corresponding one of the pixel electrodes, and a corresponding one of the gate lines respectively, and being turned ON or OFF by the gate signal").

Watanabe does not appear to explicitly specify an index B given by B=Lst/Lgd equal to or greater than 7, where a periphery length of the storage capacitor is Lst and a periphery length of a gate electrode to pixel electrode capacitor which is a capacitor formed between the gate electrode of the pixel transistor and the pixel electrode, is Lgd.

Park teaches a storage capacitor in a liquid crystal display wherein the storage capacitor has a structure for increasing the capacitance of a storage capacitor thereby improving image quality of the liquid crystal display device, reducing flicker, and reducing other image defects (ABS, entire patent). In Park, the structure of the storage capacitor is detailed in Figure 4 of Park. See also Columns 3 and 4 of Park.

Park (Figure 1) shows that the pixel electrode (17) comprises drain electrode (12D) and the periphery of the overlap of gate electrode (11G) can be seen as illustrated in Figure 1 to be much less than 1/7 of the periphery of Applicant's Lst; thereby satisfying Applicant's equation for "B."

Park is evidence to ordinary workers in the field of liquid crystals that when area and capacitance of a storage capacitor electrode is increased, image quality of an LCD display device is improved by reducing flickering and other image defects that are caused by fluctuations in the liquid crystal voltage (Park, Column 3, Lines 6-11). One of ordinary skill in the art would have had the reason, suggestion, and motivation to optimize periphery length of a storage capacitor electrode to gate electrode to improve display quality, reduce flicker, and reduce other image defects. The optimization of periphery length of storage capacitor to gate electrode periphery is a results effective variable for reducing flicker. Optimization of a results effective variable requires only routine skill in the art (MPEP 2144.05 II).

Therefore, it would have been obvious to one of ordinary skill in the art of liquid crystals at the time the invention was made to modify Watanabe in view of Park for an active matrix liquid crystal display element that has increased storage capacitance for the purpose of improving display quality, reducing flicker, and reducing other display defects as noted.

Please furthermore note that, in considering the disclosure of a reference, it is proper to take into account not only the specific teachings of the reference but also the inferences which one skilled in the art would reasonably be expected to draw therefrom (MPEP 2144.01). One of ordinary skill in the art would reasonably be expected to infer that optimizing the ratio Lst/Lgd and Lst/Lon (Applicant's claim 3) would reduce flicker, improve display quality, and reduce other image defects.

Response to Arguments

Applicant's arguments filed May 27, 2004 have been fully considered but they are not persuasive.

Applicant has argued that claims 8, 16, 18, and 20 are generic and that Applicant's election dated October 30, 2003 indicated that at least claims 1-3 are readable on the particular elected species in addition to the claims already indicated by the Examiner as being generic. This is not correct. Upon careful review of Applicant's election of claims 1-3 per Paper of October 30, 2003, it is noted that election was made without traverse and presented no indication of further generic claims. Furthermore, the Examiner did not definitely state that in fact claims 8, 16, 18, and 20 are generic.

With reference to the 112 rejections (claim objections), the Examiner noted the following in the prior Office Action with respect to the periphery length (Lgd) of the gate electrode to pixel electrode capacitor: "The periphery length, Lgd, because it is not adequately defined, may mean any number of possibilities: (1) it may mean the periphery length of the gate electrode section opposed by source and drain electrodes of a thin film transistor, or (2) it may mean the periphery

length of the gate electrode section opposed by source and drain electrodes of a thin film transistor in addition to the periphery (or periphery length) of the pixel electrode, or (3) it may mean a cross sectional length of a combination of possibilities (1) and (2) above." (Office Action of January 5, 2004 at Page 3).

Applicant claims a numeric value $B \geq 7$ (where "B" = Lst/Lgd). The Examiner finds it impossible to arrive at numeric values for "B" because a definition for "Lgd" is not provided by the Applicant.

Referring to Figure 3, in addition to the above, there is no peripheral length of the gate electrode that overlaps with the pixel electrode. Similarly, there is no peripheral length of the pixel electrode that overlaps with the gate electrode – unlike Lst. Therefore, the Examiner cannot ascertain Lgd in light of Lst.

Where Applicant has claimed a numeric ratio ("B") that relates to lengths of storage capacitor and gate electrode to pixel electrode capacitor, the lengths must be clearly defined.

Because the Examiner cannot presently meaningfully determine what "Lgd" means with clarity, the Examiner remains presently unable to give meaningful weight to that claimed ratio "B." The Examiner has, based on the Examiner's interpretation, given the best weight possible to said limitation based on the current prior art of record.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeanne A. Di Grazio whose telephone number is (571)272-2289. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Kim, can be reached on (571)272-2293. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Patent Examiner
Art Unit 2871

JDG

TOAN TON
PRIMARY EXAMINER